

ABSTRACT OF THE DISCLOSURE

A host interface includes transition detection circuitry, transition phase averaging circuitry, and bit stream sampling circuitry. The transition detection circuitry receives an incoming bit stream and a reference clock signal and detects transitions of the incoming
5 bit stream with respect to the reference clock signal. The transition detection circuitry also determines relative phases of the transitions with respect to the reference clock signal. The transition phase averaging circuitry determines an average relative phase of the detected transitions with respect to the reference clock signal and also determines, based upon the average relative phase of the detected transitions with respect to the
10 reference clock signal, a sampling phase with respect to the reference clock signal. The bit stream sampling circuitry samples the incoming bit stream at the sampling phase with respect to the reference clock signal to extract the bit values. The incoming bit stream may comply with the Universal Serial Bus 2.0 interface standard.